What is claimed is:

1. A semiconductor memory device comprising:

a first insulating layer having a gate electrode on a semiconductor substrate;

a second insulating layer formed on the first insulating layer, the second insulating layer having bit lines covered with bit line isolation layers, buried contact plugs formed between the bit lines, and a first metal contact plug connected to the semiconductor substrate through the first insulating layer;

a silicon nitride layer on the second insulating layer; and

a third insulating layer formed on the silicon nitride layer, the third insulating layer having a second metal contact plug connected to the first metal contact plug through the silicon nitride layer.

2. The device of claim 1, wherein the second insulating layer further comprises a first landing stud connected to the gate electrode through the first insulting layer.

3. The device of claim 2, wherein the bit lines comprise a direct contact plug under one of the bit line.

4. The device of claim 3, wherein the first landing stud is simultaneously formed with the direct contact plug.

5. The device of claim 2, wherein the second insulating layer further comprises a second landing stud on the first landing stud.

6. The device of claim 5, wherein the second landing stud is larger in surface area than the first landing stud.

7. The device of claim 1, wherein the first metal contact plug and the buried contact plugs are simultaneously formed with an electrical conducting material.

8. The device of claim 7, wherein the electrical conducting material includes tungsten (W).

9. The device of claim 1, wherein the third insulating layer further comprises a metal-insulator-metal capacitor on the buried contact plug.

10. A method of fabricating a semiconductor memory device, comprising the steps of:

forming a gate electrode on a silicon substrate, the silicon substrate being divided into a cell area and a peripheral area, and the gate electrode having a gate and a gate spacer being covered with the gate;

forming a first inter-layer dielectric layer (ILD1) on the silicon substrate having the gate electrode;

forming a cell pad poly between the gate electrodes in the cell area;

forming a direct contact plug (DC) on the cell pad poly in the cell area, and a first landing stud on the gate in the peripheral area;

forming a bit line on the DC in the cell area and a second landing stud on the first landing stud, the bit line being covered with a bit line isolation layer;

forming a second inter-layer dielectric layer (ILD2) on the ILD1 having the bit line to cover the bit line isolation layer;

forming a silicon nitride layer on the ILD2;

patterning the silicon nitride layer;

etching out a portion of the ILD2 in the cell area using the patterned silicon nitride layer and the bit line isolation layer as etching blocking layers until the cell pad poly is exposed, and simultaneously etching out a portion of the ILD2 and a portion of the ILD1 in the peripheral area using the patterned silicon nitride layer; and

simultaneously forming a plurality of buried contact plugs in the cell area and a first metal contact plug in the peripheral area by filling electrically conducting material to the etching portions of the ILD1 and ILD2.

11. The method of claim 10, wherein the cell pad poly is impurity doped polysilicon.

12. The method of claim 10, wherein the DC and the first landing stud includes tungsten (W).

13. The method of claim 10, wherein the bit line and the second landing stud includes tungsten (W).

14. The method of claim 10, wherein the plurality of buried contact plugs and the first metal contact plug are formed of tungsten (W).

15. The method of claim 10, wherein the silicon nitride layer is formed of Si_3N_4.

16. The method of claim 10, wherein the second landing stud is larger in surface area than the first landing stud.

17. The method of claim 10, further comprising the step of planarizing the ILD2 before forming the silicon nitride layer.

18. The method of claim 10, further comprising the steps of:

forming a third inter-layer dielectric layer (ILD3) on the silicon nitride layer;

patterning the ILD3 to expose the buried contact plug; and

forming a metal-insulator-metal (MIM) capacitor on the buried contact plug.

19. The method of claim 18, further comprising the step of planarizing the ILD3 before forming the patterning the ILD3.

20. The method of claim 19, wherein the step of forming the MIM capacitor comprises the steps of:

forming a storage electrode on the silicon nitride layer;

forming a insulating layer on the storage electrode; and

forming a floating electrode on the insulating layer.

21. The method of claim 20, wherein the storage electrode is formed of tungsten (W).

22. The method of claim 18, further comprising the steps of:

forming a fourth inter-layer dielectric layer (ILD4) on the ILD3 having the MIM capacitor;

patterning a portion of ILD4 and a portion of ILD3 to expose the MC0, patterning a portion of the ILD4, a portion of ILD3, and a portion of ILD2 to expose the second landing stud, and patterning a portion of the ILD4 to expose the MIM capacitor; and

forming a second metal contact plug to connect to the MC0, the second landing stud, and MIM capacitor.

23. The method of claim 22, wherein the second metal contact plug is formed of tungsten.